

CLAIMS

WHAT IS CLAIMED IS:

- 1 1. A method of manufacturing an integrated circuit having a
2 gate structure above a substrate including germanium, the method
3 comprising:
4 forming a first layer above the gate structure and above the
5 substrate;
6 forming a second layer above the first layer; and
7 doping source and drain regions through the first layer and
8 the second layer, whereby germanium back sputtering is reduced.
- 1 2. The method of claim 1, further comprising:
2 annealing the substrate whereby the first layer and the
3 second layer prevent outgassing.
- 1 3. The method of claim 1, wherein the first layer includes at
2 least one of silicon dioxide and silicon carbide.
- 1 4. The method of claim 1, wherein second layer includes at
2 least one of silicon nitride, titanium, titanium nitride, titanium/titanium
3 nitride, tantalum nitride, and silicon carbide.
- 1 5. The method of claim 1, wherein the steps of forming a first
2 layer and forming a second layer utilize low temperature deposition.
- 1 6. The method of claim 5, wherein the low temperature
2 deposition is performed at a temperature below approximately 800°C.
- 1 7. The method of claim 5, wherein the low temperature
2 deposition is a chemical vapor deposition process.

1 8. The method of claim 1, further comprising:
2 providing a rapid thermal anneal.

1 9. A method of forming source and drain regions in a strained
2 semiconductor layer, the method comprising:
3 providing a first layer comprising at least one of silicon
4 nitride and silicon dioxide above the strained semiconductor layer;
5 providing a second layer above the first layer, the second
6 layer containing nitrogen, titanium, tantalum, or carbon;
7 implanting non-neutral dopants into the strained
8 semiconductor layer; and
9 annealing the strained semiconductor layer.

1 10. The method of claim 9, wherein the annealing step is a rapid
2 thermal anneal for activating the dopants.

1 11. The method of claim 10, further comprising:
2 removing the second layer after the annealing step.

1 12. The method of claim 9, further comprising:
2 providing an insulative material above the first layer.

1 13. The method of claim 12, wherein the first layer includes
2 silicon dioxide and the insulative material includes silicon nitride.

1 14. The method of claim 9, wherein the anneal is a rapid thermal
2 anneal at a temperature above 600°C.

1 15. The method of claim 14, wherein the first layer is deposited
2 in a low temperature process.

1 16. The method of claim 15, wherein the layer containing
2 titanium, nitrogen, tantalum or carbon is provided in a low temperature
3 process.

1 17. A method of fabricating a transistor in a germanium
2 containing layer, the method comprising:
3 providing a gate structure above the germanium containing
4 layer;
5 providing a first layer of insulative material in a low
6 temperature process above the germanium containing layer;
7 doping the germanium containing layer to form source and
8 drain regions; and
9 annealing the germanium containing layer to activate dopants
10 in the source and drain regions.

1 18. The method of claim 17, wherein the step of providing a first
2 layer is an LPCVD deposition process performed at a low temperature.

1 19. The method of claim 18, wherein the step of providing a first
2 layer utilizes an oxygen atmosphere and silane atmosphere.

1 20. The method of claim 19, further comprising:
2 depositing a second layer over the first layer before the
3 doping step.